an execution step in which, on the basis of the control commands and the step-up signals, the memory system:

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controls access to the plurality of memory circuits by the first and second processors in an asynchronous manner.

REMARKS

Claims 1-5 remain pending in this application. Claims 1-5 have been amended. Favorable reconsideration is respectfully requested.

In the Office Action, Claims 1-5 were rejected under 35 U.S.C. 102 as being anticipated by U.S. Patent 4,734,850 (Torii et al.)

Applicant respectfully submits that the rejected claims as amended are patentable for at least the following reasons.

Claim 1 has been amended to recite that a control unit includes at least two counters that can be externally loaded, respectively, by signals from first and second processors. The control unit, on the basis of control commands and the signals, controls access to a memory system by the first and second processor in an asynchronous manner.

Support for this feature can at least be found in Fig. 2 and page 5, lines 7-9 and lines 29-33, of the specification.

Torii et al., as read by Applicant, does not teach or suggest these features as recited in Claim 1. For example, while Torii et al. may be deemed to show write and read counters, nothing found in Torii et al. teaches that such counters are externally loaded by signals from first and second processors. In addition, while Torii et al. may also be

deemed to show a write and a read request input, nothing found in Torii et al. teaches that first and second processors can access a memory system in an asynchronous manner.

At least for the above reasons, Claim 1 is believed patentable over Torii et al.

Independent Claims 4 and 5 recite a similar feature as discussed above in regard to Claim 1, and are believed allowable for at least similar reasons.

A review of the other art of record has failed to reveal anything which, in Applicant's opinion, would remedy the deficiencies of the art discussed above, as reference a against the independent claims. Those claims are therefore believed patentable over the art of record.

The other rejected claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the same reasons. In addition, however, each dependent claim is also deemed to define an additional aspect of the invention, and should be individually considered on its own merits.

This Amendment After Final Rejection is believed clearly to place this application in condition for allowance and its entry is therefore believed proper under 37 C.F.R. § 1.116. In any event, however, entry of this Amendment After Final Rejection, as an earnest effort to advance prosecution and reduce the number of issues, is respectfully requested.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

Applicant's undersigned attorney may be reached by telephone at the number given below.

Respectfully submitted,

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On April 26, 2003

By _____
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Appendix of Marked-up Claims

1. (Amended) A data processing arrangement comprising:

a first processor for providing successive sets of input data;

a second processor for receiving successive sets of output data;

a memory system including a plurality of memory circuits where all of the plurality of memory circuits are accessible by the first processor and the second processor;

a master controller for setting up the plurality of memory circuits of said memory system using control commands associated with a set of input data and a set of output data; and

a control unit ~~for, on the basis of the control commands, ensuring that input data and output data are not simultaneously required for writing and reading from one of the plurality of independent memory circuits~~including at least two counters that can be externally loaded, respectively, by signals from the first and second processors, the control unit, on the basis of the control commands and the signals, controls access to the memory system by the first and second processor in an asynchronous manner.

2. (Amended) A data processing arrangement, as claimed in claim 1, wherein the ~~control unit comprises:~~at least two counters includes:

a write-counter whose value is modified in association with the data received from the set of input data and which value indicates the write-address of the data in the first memory circuit; and

a read-counter whose value is modified in association with the data provided from

the set of output data and which value indicates the read-address of the data in the second memory circuit.

3. (Amended) A data processing arrangement, as claimed in claim 1, wherein the control unit ~~comprises~~ includes a write-input port for receiving a write-data signal from the first processor in response to which the control unit generates the write-address and the control unit further comprises a read-input port for receiving a read-data signal from the second processor in response to which the control unit generates the read-address.

4. (Amended) A memory system comprising:

a plurality of memory circuits for receiving successive sets of input data and for providing successive sets of output data, all of the plurality of memory circuits being accessible by at least two processors;

a control unit including at least two counters that can be externally loaded, respectively, by signals from the at least two processors, and being programmable by means of control commands and the signals ~~associated with a set of input data and a set of output data and, on the basis of these control commands, for ensuring that input data and output data are not simultaneously required for writing and reading from one of the plurality of memory circuits~~, controls access to the plurality of memory circuits by the at least two processors in an asynchronous manner.

5. (Amended) A method of processing data in a data processing arrangement including a first processor for providing successive sets of input data, a second processor for receiving successive sets of output data and a memory system including a plurality of

memory circuits that are all accessible by both the first and processor and the second processor for receiving the successive sets of input data and providing the successive sets of output data,

the method comprising, for a set of input data and a set of output data, the following steps:

a configuration step in which the memory system is set up by means of control commands associated with the set of input data and the set of output data;

a counter set-up step in which at least two counters receive step-up signals, respectively, from the first and second processor; and

an execution step in which, on the basis of the control commands and the step-up signals, the memory system:

~~ensures~~ controls ~~that input data and output data are not simultaneously required for writing and reading from one of~~access to the plurality of memory circuits by the first and second processors in an asynchronous manner.